


CLOCK GRID SKEW REDUCTION USING A WIRE TREE ARCHITECTURE

Abstract

 An integrated circuit having a clock driver connected to a non-peripheral region of a clock grid is provided. Providing interconnect that connects a clock driver to non-peripheral regions of the clock grid effectively leads to reduced clock skew due to reduced RC delays from clock grid connection points to components operatively connected to the clock grid. Further, a method for reducing clock skew on a clock grid using a wire tree architecture structure is provided.

22752_1

22752_1